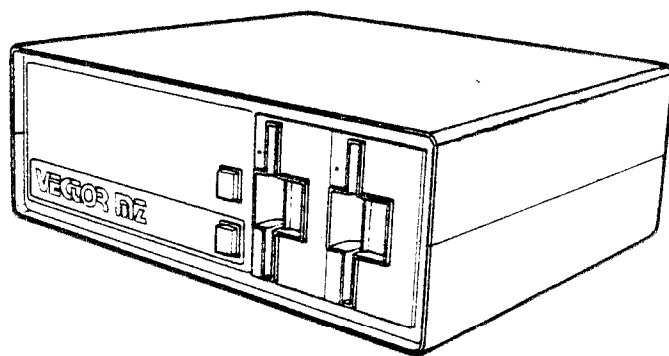
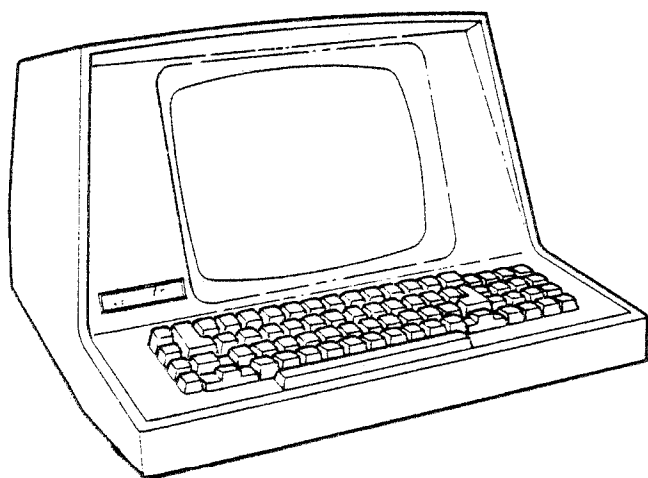


8K STATIC RAM

USERS MANUAL



VECTOR
VECTOR GRAPHIC, INC.

REPAIR AGREEMENT

The 8K Memory Board sold hereunder is sold "as is", with all faults and without any warranty, either expressed or implied, including any implied warranty of fitness for intended use or merchantability. However, the above notwithstanding, VECTOR GRAPHIC, INC., will, for a period of ninety (90) days following delivery to customer, repair or replace any 8K Memory Board that is found to contain defects in materials or workmanship, provided:

1. Such defect in material or workmanship existed at the time the 8K Memory Board left the VECTOR GRAPHIC, INC., factory;
2. VECTOR GRAPHIC, INC., is given notice of the precise defect claimed within ten (10) days after its discovery;
3. The 8K Memory Board is promptly returned to VECTOR GRAPHIC, INC., at customer's expense, for examination by VECTOR GRAPHIC, INC., to confirm the alleged defect, and for subsequent repair or replacement if found to be in order.

Repair, replacement or correction of any defects in material or workmanship which are discovered after expiration of the period set forth above will be performed by VECTOR GRAPHIC, INC., at Buyer's expense, provided the 8K Memory Board is returned, also at Buyer's expense, to VECTOR GRAPHIC, INC., for such repair, replacement or correction. In performing any repair, replacement or correction after expiration of the period set forth above, Buyer will be charged in addition to the cost of parts the then-current VECTOR GRAPHIC, INC., repair rate. At the present time the applicable rate is \$35.00 for the first hour, and \$18.00 per hour for every hour of work required thereafter. Prior to commencing any repair, replacement or correction of defects in material or workmanship discovered after expiration of the period for no-cost-to-Buyer repairs, VECTOR GRAPHIC, INC., will submit to Buyer a written estimate of the expected charges, and VECTOR GRAPHIC, INC., will not commence repair until such time as the written estimate of charges has been returned by Buyer to VECTOR GRAPHIC, INC., signed by duly authorized representative authorizing VECTOR GRAPHIC, INC., to commence with the repair work involved. VECTOR GRAPHIC, INC., shall have no obligation to repair, replace or correct any 8K Memory Board until the written estimate has been returned with approval to proceed, and VECTOR GRAPHIC, INC., may at its option also require prepayment of the estimated repair charges prior to commencing work.

Repair Agreement void if the enclosed card is not returned to VECTOR GRAPHIC, INC. within ten (10) days of end consumer purchase.

8K RAM BOARD

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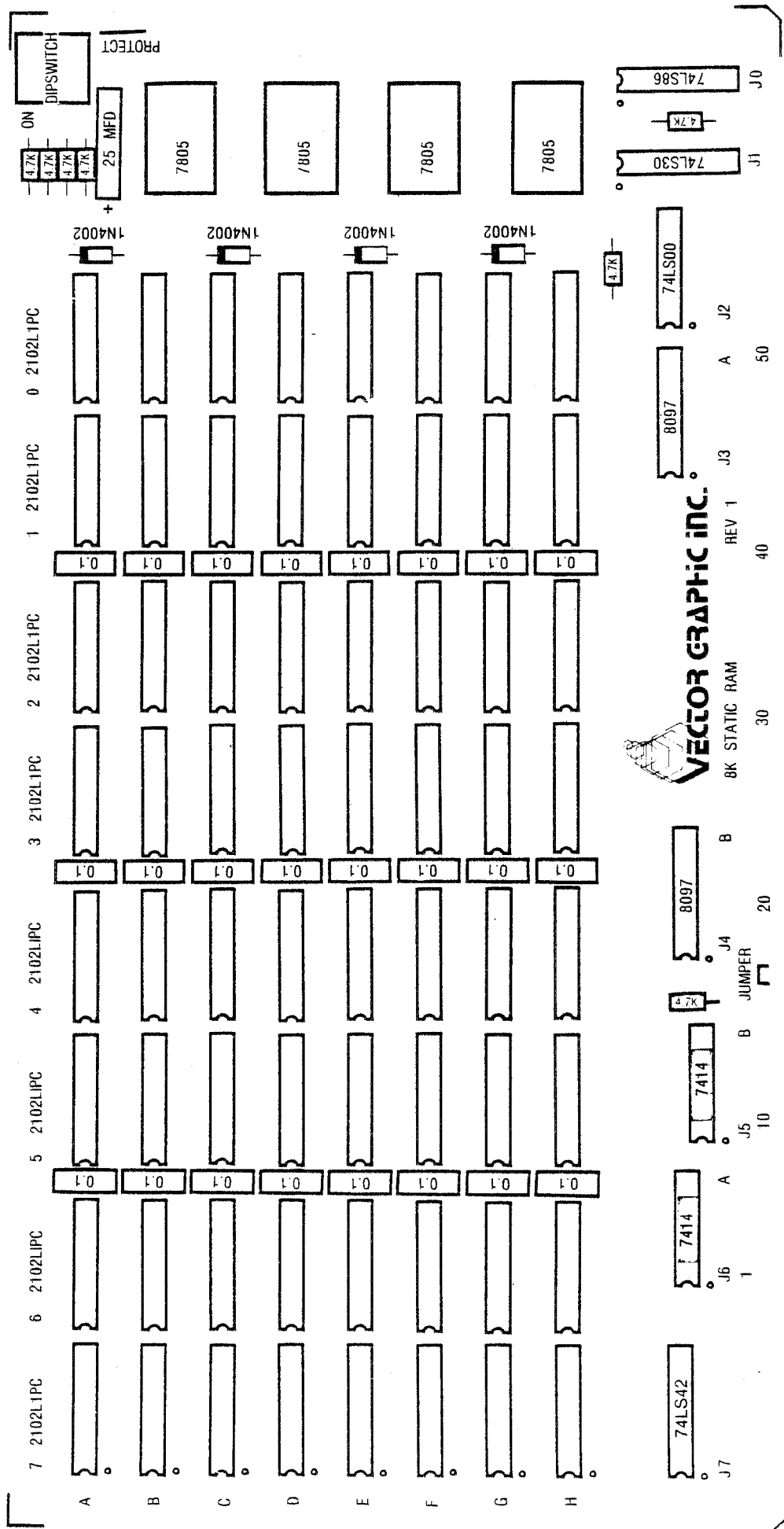
INTRODUCTION

THE VECTOR GRAPHIC 8K STATIC MEMORY BOARD IS DESIGNED TO BE PLUG-IN COMPATIBLE WITH YOUR VECTOR 1, ALTAIR, IMSAI AND POLY 88 SYSTEMS. WE HAVE PROVIDED A HIGH QUALITY PRODUCT BY USING THE FINEST AVAILABLE MEMORY CHIPS AND AEROSPACE QUALITY PRINTED CIRCUIT BOARD. THE MEMORY OPERATES AT THE MAXIMUM SPEED OF 8080A MPU OR Z-80 MPU CAPACITY WITH NO WAIT STATES REQUIRED. THE MEMORY CHIP ADDRESS INPUTS ARE BUFFERED TO REDUCE THE CAPACITANCE LOADING ON THE ADDRESS BUS, A MAJOR PLUS SINCE THIS COULD EXCEED 2000 PF IN A LARGE SYSTEM. ADDRESS SELECTION IS BY MEANS OF A DIP SWITCH LOCATED ON THE UPPER EDGE OF THE BOARD. WITH THIS FEATURE YOU MAY CHANGE THE BOARD ADDRESS FOR PROGRAMS THAT RUN IN HIGH MEMORY WITHOUT HAVING TO REMOVE THE BOARD FROM THE COMPUTER. ANOTHER CONVENIENCE IS THE OUTPUT DISABLE FEATURE WHICH PERMITS START UP OF THE COMPUTER WITHOUT THE FRONT PANEL SWITCHES. FURTHER, THE BOARD CAN BE WRITE PROTECTED. TYPICAL POWER CONSUMPTION OF THE 250 NS BOARD IS 1.6 AMPS USING FAIRCHILD 2102LHPC CHIPS.

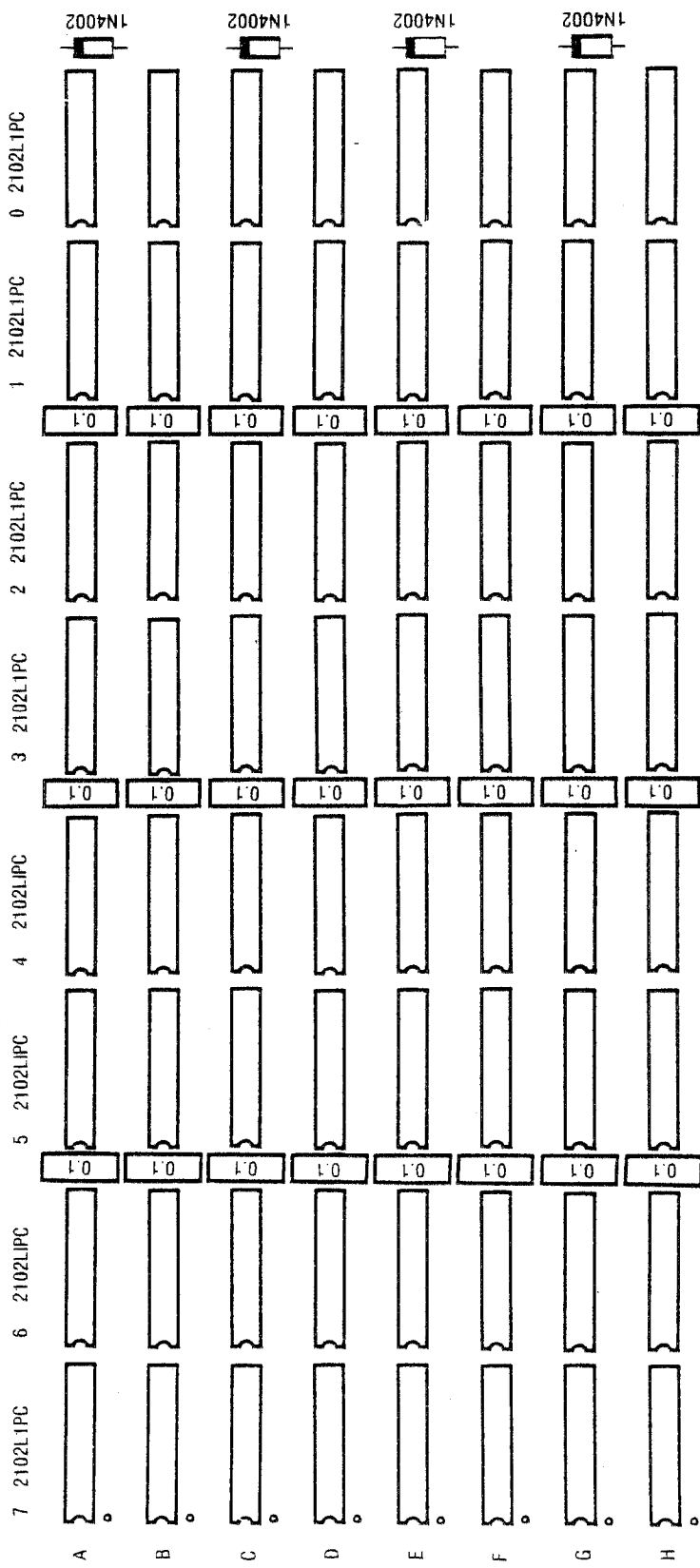
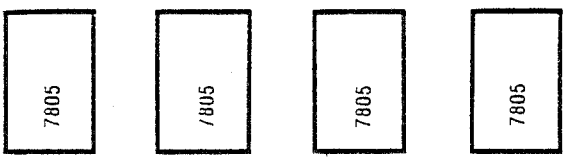
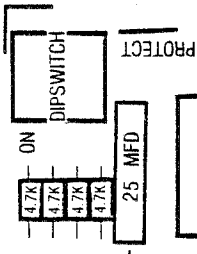
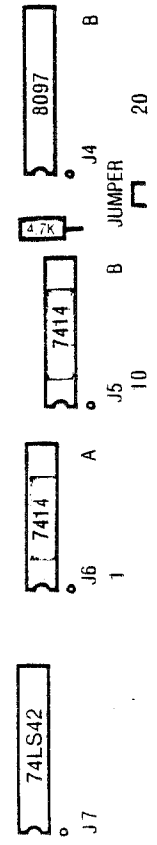
IF THERE IS ANYTHING THAT YOU DO NOT UNDERSTAND, PLEASE DO NOT HESITATE TO CALL OR WRITE US!

PARTS LIST

<u>QTY.</u>	<u>DESCRIPTION</u>
1	PRINTED CIRCUIT BOARD
64	2102LHPC STATIC RAMS OR EQUIVALENT
1	4-POSITION DIP SWITCH
4	7805 REGULATORS
4	SETS OF HARDWARE FOR THE REGULATORS 6-32X3/8" SCREWS, NUTS AND LOCKWASHERS
2	74367/8097 TRI-STATE BUS DRIVERS
2	7414 SCHMITT TRIGGERS
1	74LS42 ONE OF EIGHT DECODER
1	74LS86 EXCLUSIVE OR GATE
1	74LS30 8 INPUT NAND GATE
1	74LS00 QUAD 2 INPUT NAND GATE
1	22 MFD 16 VOLT AXIAL ELECTROLYTIC CAPACITOR
24	0.1 MFD 50 VOLT MONOLITHIC RADIAL CAPACITORS
1	470 PF 50 VOLT AXIAL CERAMIC CAPACITOR
7	4.7K RESISTORS 1/4 WATT (BANDS OF YELLOW, VIOLET, RED)
4	IN4002 DIODES
5	14 PIN IC SOCKETS
67	16 PIN IC SOCKETS
4	THERMALLOY #6073B HEAT SINKS

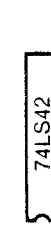
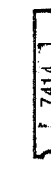
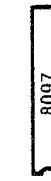
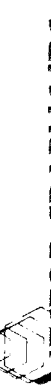
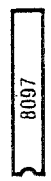


VECTOR GRAPHIC INC.
 8K STATIC RAM



7 2102L1PC 6 2102L1PC 5 2102L1PC 4 2102L1PC 3 2102L1PC 2 2102L1PC 1 2102L1PC 0 2102L1PC

A B C D E F G H



J0 J1 J2 J3 J4 J5 J6 J7
 A B
 REV 1
 40 50

USERS GUIDE

POWER SUPPLY CONSIDERATIONS

FOR RELIABLE OPERATION, AN ADEQUATE, UNREGULATED 8 VOLT SUPPLY MUST BE PROVIDED. THE REGULATORS ON THE 8K BOARD REQUIRE AT LEAST 2 VOLTS DROP TO REGULATE PROPERLY. THIS MEANS THAT THE TROUGH OF THE UNREGULATED SUPPLY WAVEFORM MUST BE AT LEAST 7 VOLTS. TO ALLOW FOR NORMAL LINE VOLTAGE FLUCTUATIONS, AT LEAST 10% MARGIN SHOULD BE MAINTAINED ABOVE THIS. THUS WITH 1 VOLT PEAK-PEAK RIPPLE, THE AVERAGE UNREGULATED SUPPLY VOLTAGE SHOULD BE AT LEAST 8.2 VOLTS. TO MAINTAIN LESS THAN 1 VOLT P-P RIPPLE, AT LEAST 8000 MFD OF FILTER CAPACITANCE SHOULD BE PROVIDED PER AMPERE OF TOTAL CURRENT DRAIN. IF YOUR COMPUTER SUPPLY IS NOT ADEQUATE, WE OFFER A REPLACEMENT POWER TRANSFORMER WHICH WILL PRODUCE +8V, 18A; $\pm 16V$, 2.5A. CONTACT US FOR FURTHER INFORMATION.

LINE TRANSIENTS

MOST OF US HAVE EXPERIENCED THE FRUSTRATION OF SPENDING A LOT OF TIME WORKING ON A PROGRAM, ONLY TO HAVE A POWER LINE TRANSIENT CAUSE THE PROGRAM TO BOMB. THIS PROBLEM IS USUALLY DUE TO HIGH FREQUENCY TRANSIENTS CAUSED BY MOTOR STARTING CONTACTORS OR INDUCTIVE ENERGY STORAGE SOMEWHERE ON THE POWER DISTRIBUTION SYSTEM. ACTUAL POWER OUTAGES ARE RELATIVELY RARE. MEMORY WRITE PROTECTION OR STANDBY POWER SOURCES WILL NOT PREVENT THIS PROBLEM. IT IS RECOMMENDED THAT A POWER LINE FILTER BE INSTALLED IN YOUR COMPUTER AS CLOSE TO THE LINE CORD ENTRY POINT AS POSSIBLE. A CORCOM MODEL 3B1 OR EQUIVALENT IS VERY EFFECTIVE. VECTOR GRAPHIC SYSTEMS HAVE A POWER LINE FILTER AS STANDARD EQUIPMENT.

VENTILATION

IT IS RECOMMENDED THAT ADEQUATE FORCED VENTILATION BE PROVIDED IN ENCLOSED CABINETS. IF THE COMPUTER IS OPERATED WITHOUT A COVER, ALLOW 2 SLOTS SEPARATION OR 1.5" BETWEEN BOARDS. IF YOU CAN'T HOLD YOUR FINGER ON THE HEAT SINK FOR AT LEAST A FEW SECONDS, THE VENTILATION IS NOT ADEQUATE.

ADDRESS SELECTION

THE ADDRESS RANGE THAT THE BOARD RESPONDS TO IS SELECTED BY THE THREE LEFT SWITCHES ON THE DIP SWITCH. THEY ARE ARRANGED IN EXACTLY THE SAME CONFIGURATION AS THE MOST SIGNIFICANT FRONT PANEL ADDRESS SWITCHES; NAMELY A 15, THE MOST SIGNIFICANT ADDRESS BIT, IS ON THE LEFT, AND SETTING THE SWITCH TO THE ON, OR UP, POSITION SETS THE ADDRESS BIT HIGH. TABLE 1 GIVES THE SWITCH SETTING FOR ALL POSSIBLE ADDRESS RANGES.

TABLE 1

ADDRESS RANGE	SWITCH SETTING (1=ON)
0000-1FFF	000X
2000-3FFF	001X
4000-5FFF	010X
6000-7FFF	011X
8000-9FFF	100X
A000-BFFF	101X
C000-DFFF	110X
E000-FFFF	111X

IF YOU HAVE 4K OR SMALLER BOARDS, THE MOST CONVENIENT ARRANGEMENT IS TO PUT THE 8K BOARDS AT THE LOWEST ADDRESS FOLLOWED BY THE 4K AND SMALLER BOARDS. IF YOU HAVE MACHINE LANGUAGE ROUTINES ON PROMS THAT USE THE STACK, A SMALL MEMORY BOARD LOCATED JUST BELOW 32K IS VERY CONVENIENT. THIS ALLOWS YOU TO ADD TO YOUR MAIN MEMORY WITHOUT HAVING TO REPROGRAM PROMS WITH THE NEW STACK LOCATION.

MEMORY WRITE PROTECT

THE RIGHT HAND DIP SWITCH CONTROLS THE MEMORY WRITE PROTECT. WITH THE SWITCH OFF, THE MEMORY CAN NOT BE WRITTEN INTO. THE NORMAL POSITION IS ON. THIS FEATURE IS NOT USED WHEN RUNNING BASIC, BUT CAN BE USED TO PROTECT SOURCE FILES OR ASSEMBLERS WHEN DEBUGGING MACHINE CODE ROUTINES, WHICH OFTEN GO AWRY AND CAUSE OTHER PARTS OF MEMORY TO BE ALTERED. TO USE THE FEATURE, MERELY FLIP THE PROTECT SWITCH DOWN BEFORE EXECUTING THE MACHINE USAGE ROUTINE. NATURALLY, THE STACK OR MEMORY LOCATIONS ALTERED DURING NORMAL PROGRAM EXECUTION CAN NOT RESIDE ON PROTECTED BOARDS.

OUTPUT DISABLE FEATURE

THERE IS ONE JUMPER LOCATION, AS SHOWN ON THE COMPONENT PLACEMENT DIAGRAM, WHICH PERMITS THE TRI-STATE BUS DRIVERS TO BE DISABLED DURING MEMORY READ CYCLES. THIS PERMITS A TRANSPARENT BOOTSTRAP LOADER TO BE IMPLEMENTED USING COMPONENTS ON OTHER BOARDS. WITH THE JUMPER INSTALLED, PULLING LINE 67 ON THE BUS LOW WILL DISABLE THE TRI-STATE BUS DRIVERS.

MEMORY TEST PROGRAM

THERE ARE NUMEROUS MEMORY TEST PROGRAMS AVAILABLE IN THE LITERATURE FOR ANY LEVEL OF SYSTEM SOPHISTICATION. IF YOU HAVE 8K BASIC UP AND RUNNING, OR KNOW SOMEONE WHO DOES, THE FOLLOWING PROGRAM WILL DO A THOROUGH JOB OF TESTING YOUR MEMORY WITH A RANDOM PATTERN USING THE RND FUNCTION. TO USE THE PROGRAM, A SYSTEM WITH AT LEAST 8K OF MEMORY IS REQUIRED, NOT COUNTING THE BOARD TO BE TESTED. SET THE BOARD ADDRESS TO SOME RANGE ABOVE THE EXISTING MEMORY BUT BELOW 32K. LOAD BASIC AND INITIALIZE MEMORY AT 8192 BYTES, SO BASIC WILL NOT LOAD A PROGRAM IN THE BOARD TO BE TESTED. LOAD THE TEST PROGRAM USING THE KEYBOARD, PAPER TAPE, OR CASSETTE. RUN THE PROGRAM AND ENTER THE STARTING AND ENDING

MEMORY LOCATIONS TO BE TESTED (IN DECIMAL). IT TAKES SEVERAL MINUTES TO TEST A BOARD, AFTER WHICH THE PROGRAM TYPES "CHECK OK" AND CONTINUES TESTING. A THOROUGH TEST REQUIRES ABOUT 10 PASSES. IF AN ERROR OCCURS, THE LOCATION IS PRINTED OUT ALONG WITH THE NUMBER WRITTEN INTO MEMORY AND READ FROM MEMORY.

PROGRAM LISTING (MITS BASIC)

```

30 INPUT "HIGH MEMORY ADD.":H
70 INPUT "LOW MEMORY ADD.":L
121 PRINT "LOCATION", "WROTE", "READ"
122 A=RND(1)
125 B=RND(-A)
130 FOR N=L TO H
140 POKE N,INT(256*RND(1))
150 NEXT
160 B=RND (-A)
170 FOR N=L TO H
180 IF PEEK(N)=INT(256*RND(1)) ) GOTO 200
190 PRINT N,INT(256*RND(0)),PEEK(N)
200 NEXT
210 PRINT "CHECK OK"
220 GOTO 122
OK

```

EXAMPLE RUN

```

RUN
HIGH MEMORY ADD.? 20479
LOW MEMORY ADD.? 8192
LOCATION          WROTE          READ
CHECK OK
CHECK OK
CHECK OK

```

MACHINE LANGUAGE TEST PROGRAM

THE MACHINE LANGUAGE MEMORY TEST PROGRAM ON THE FOLLOWING PAGES IS ABSTRACTED FROM THE VECTOR 1 MONITOR PROGRAM, AND ASSEMBLED TO RUN IN THE LOWEST 256 BYTES OF MEMORY. START EXECUTION AT ADDRESS 0000H. A "*" WILL BE TYPED IF YOU HAVE PROPERLY PATCHED THE I/O ROUTINES FOR YOUR SYSTEM. PTCN IS THE OUTPUT ROUTINE FOR A 3P+S BOARD WITH STATUS INVERTED (OR MITS REV. 1 SIO). RDCN IS THE INPUT ROUTINE. IF YOU ARE USING A BOARD WITH A PROGRAMMABLE USART, YOU WILL HAVE TO INITIALIZE IT IN ADDITION TO CHANGING THE MASK, JUMP CONDITION, AND PORT.

AFTER "*", TYPE IN FOUR HEX CHARACTERS FOR THE STARTING ADDRESS OF THE MEMORY BLOCK TO BE TESTED AND FOUR HEX CHARACTERS FOR THE ENDING ADDRESS OF THE BLOCK. SPACE IS AUTOMATIC, AND IF YOU TYPE ANY CHARACTERS OTHER THAN 0-9, A-F THE PROGRAM WILL DO STRANGE THINGS. A RESET WILL TERMINATE THE TEST. THE PROGRAM GENERATES A 2 16-1 BYTE PSEUDO-RANDOM NUMBER SEQUENCE, WRITES A PORTION OF IT IN THE BLOCK OF MEMORY AND THEN REGENERATES THE SEQUENCES FROM THE SAME POINT TO COMPARE WITH WHAT IS READ FROM MEMORY. IF THE PASS IS CORRECT, A NEW PORTION OF THE SEQUENCE IS WRITTEN INTO MEMORY. ERRORS ARE PRINTED OUT WITH THE ADDRESS, WHAT WAS WRITTEN, AND WHAT WAS READ. USE THE ADDRESS LOCATIONS ON THE COMPONENT PLACEMENT DIAGRAM TO LOCATE THE BAD ROW, AND THE INCORRECT BIT TO LOCATE THE COLUMN. AN OUTPUT OF "FF" MEANS NO MEMORY. MORE THAN ONE BIT WRONG IS USUALLY CAUSED BY CHIPS IN BACKWARDS (WHICH DOES NOT DESTROY THE MEMORY CHIPS, CONTRARY TO TTL) OR A SOLDER BRIDGE. BENT UNDER ADDRESS PINS CAUSE MANY ERRORS TO BE PRINTED OUT IN ONE 1K BLOCK.

THE MOST DIFFICULT PROBLEM TO ISOLATE IS A SHORT CIRCUITED ADDRESS LINE TO THE MEMORY ARRAY. THIS WILL USUALLY CAUSE ALL MEMORY LOCATIONS TO INDICATE ERROR WITH ALL BITS BAD. THE SHORT CAN BE CAUSED BY A SOLDER BRIDGE, AN ETCH BRIDGE (ALTHOUGH EACH BOARD IS ELECTRICALLY TESTED FOR THIS), OR A DEFECTIVE CHIP. IF YOU CANNOT LOCATE THE PROBLEM VISUALLY, REMOVE HALF OF THE ROWS OF CHIPS AND TEST WITH A SMALLER BLOCK LENGTH. REPEAT THIS UNTIL ALL CHIPS HAVE BEEN ELIMINATED AS TROUBLE MAKERS. THEN TEST BETWEEN MEMORY SOCKET PINS USING A LOW

VOLTAGE OHMMETER ON THE X1 OHMS SCALE AT ONE CHIP LOCATION. IF THIS FAILS TO REVEAL THE PROBLEM, SOME EXPERIENCE IN TROUBLESHOOTING ELECTRONIC CIRCUITS BECOMES VERY USEFUL.

0000		0010	CONC	EQU	0	CONSOLE STAT PORT
0000		0020	COND	EQU	1	CONSOLE DATA PORT
0000		0050	SPTR	EQU	0100H	STACK POINTER
0000		0051	*			
0000		0052	***	VECTOR GRAPHIC MEMORY TEST PROGRAM		
0000		0053	*FOR	SIO REV. 1 AND 3P+S W. INV. STATUS		
0000		0060	* ASSEMBLED FOR 0000 TO 00FF HEX			
0000		0070	*			
0000	31 00 01	0100	START	LXI	SP,SPTR	
0003	CD 38 00	0105		CALL	CRLF	
0006	3E 2A	0110		MVI	A,'*'	PRINT "***
0008	CD 2C 00	0120		CALL	PTCN	
000B	C3 50 00	0130		JMP	TMEM	
000E		0410	*			
000E		0420	***	CONVERT UP TO 4 HEX DIGITS TO BIN		
000E		0430	*			
000E	21 00 00	0440	AHEX	LXI	H,0	GET 16 BIT ZERO
0011	0E 04	0450		MVI	C,4	COUNT OF 4 DIGITS
0013	CD 42 00	0460	AHE1	CALL	RDCN	READ A BYTE
0016	29	0470		DAD	H	SHIFT 4 LEFT
0017	29	0480		DAD	H	
0018	29	0490		DAD	H	
0019	29	0500		DAD	H	
001A	D6 30	0510		SUI	48	ASCII BIAS
001C	FE 0A	0520		CPI	10	DIGIT 0-10
001E	DA 23 00	0530		JC	ALF	
0021	D6 07	0540		SUI	7	ALPHA BIAS
0023	85	0550	ALF	ADD	L	
0024	6F	0560		MOV	L,A	
0025	0D	0570		DCR	C	4 DIGITS?
0026	C2 13 00	0580		JNZ	AHE1	KEEP READING
0029	EB	0585		XCHG		
002A	3E 20	0590	SPCE	MVI	A,20H	PRINT SPACE
002C	F5	0600	PTCN	PUSH	PSW	SAVE REG A
002D	DB 00	0610	PTLOP	IN	CONC	READ PRTR STATUS
002F	E6 80	0620		ANI	80H	IF BIT 7 NOT 0,
0031	C2 2D 00	0630		JNZ	PTLOP	WAIT TILL TIS
0034	F1	0640		POP	PSW	THEN RECOVER A
0035	D3 01	0650		OUT	COND	AND PRINT IT
0037	C9	0660		RET	RETURN	FROM PTCN
0038	3E 0D	0670	CRLF	MVI	A,0DH	PRINT CR
003A	CD 2C 00	0680		CALL	PTCN	
003D	3E 0A	0690		MVI	A,0AH	
003F	C3 2C 00	0700		JMP	PTCN	
0042		0710	*			
0042		0720	***	READ FROM CONSOLE TO REG A ***		
0042		0730	*			
0042	DB 00	0740	RDCN	IN	CONC	READ KB STATUS
0044	E6 01	0750		ANI	1	IF BIT 1 NOT 0
0046	C2 42 00	0760		JNZ	RDCN	REPEAT UNTIL IT IS
0049	DB 01	0770		IN	COND	READ FROM KB
004B	E6 7F	0780		ANI	7FH	STRIP OFF MSB
004D	C3 2C 00	0790		JMP	PTCN	ECHO ONTO PRINTER
0050		1590	*			

0050		1600	*** MEMORY TEST ROUTINE ***	
0050		1610	*	
0050	CD 0E 00	1620	TMEM CALL AHEX	READ BLK LEN
0053	CD 0E 00	1640	CALL AHEX	READ ST ADD
0056	01 5A 5A	1650	LXI B,5A5AH	INI B,C
0059	CD 81 00	1660	CYCL CALL RNDM	
005C	C5	1670	PUSH B	KEEP ALL REGS
005D	E5	1680	PUSH H	
005E	D5	1690	PUSH D	
005F	CD 81 00	1700	TLOP CALL RNDM	
0062	70	1710	MOV M,B	WRITE IN MEM
0063	CD C5 00	1720	CALL BMP	
0066	C2 5F 00	1760	JNZ TLOP	REPEAT LOOP
0069	D1	1770	POP D	
006A	E1	1780	POP H	RESTORE ORIG
006B	C1	1790	POP B	VALUES OF
006C	E5	1800	PUSH H	
006D	D5	1810	PUSH D	
006E	CD 81 00	1820	RLOP CALL RNDM	GEN NEW SEQ
0071	7E	1830	MOV A,M	READ MEM
0072	B8	1840	CMP B	COMP MEM
0073	C4 9F 00	1850	CNZ ERR	CALL ERROR ROUT
0076	CD C5 00	1860	CALL BMP	
0079	C2 6E 00	1930	JNZ RLOP	
007C	D1	1940	POP D	
007D	E1	1950	POP H	
007E	C3 59 00	1960	JMP CYCL	
0081		1970	*** THIS ROUTINE GENERATES	RANDOM NOS ***
0081	78	1980	RNDM MOV A,B	LOOK AT B
0082	E6 B4	1990	ANI 0B4H	MASK BITS
0084	A7	2000	ANA A	CLEAR CY
0085	EA 89 00	2010	JPE PEVE	JUMP IF EVEN
0088	37	2020	STC	
0089	79	2030	PEVE MOV A,C	LOOK AT C
008A	17	2040	RAL	ROTATE CY IN
008B	4F	2050	MOV C,A	RESTORE C
008C	78	2060	MOV A,B	LOOK AT B
008D	17	2070	RAL	ROTATE CY IN
008E	47	2080	MOV B,A	RESTORE B
008F	C9	2090	RET	RETURN W NEW B,C
0090		2100	*	
0090		2110	*** ERROR PRINT OUT ROUTINE	
0090		2120	*	
0090	CD 38 00	2130	PTAD CALL CRLF	PRINT CR,LF
0093	7C	2140	MOV A,H	PRINT
0094	CD AB 00	2150	CALL PT2	ASCII
0097	7D	2160	MOV A,L	CODES
0098	CD AB 00	2170	CALL PT2	FOR
009B	CD 2A 00	2180	CALL SPCE	ADDRESS
009E	C9	2200	RET	
009F	F5	2210	ERR PUSH PSW	SAVE ACC
00A0	CD 90 00	2220	CALL PTAD	PRINT ADD.
00A3	78	2230	MOV A,B	DATA
00A4	CD AB 00	2240	CALL PT2	WRITTEN
00A7	CD 2A 00	2250	CALL SPCE	
00AA	F1	2270	POP PSW	DATA READ

00AB	F5			2280	PT2	PUSH	PSW		
00AC	CD	B3	00	2290		CALL	BINH		
00AF	F1			2300		POP	PSW		
00B0	C3	B7	00	2310		JMP	BINL		
00B3	1F			2320	BINH	RAR			
00B4	1F			2330		RAR			
00B5	1F			2340		RAR			
00B6	1F			2350		RAR			
00B7	E6	0F		2360	BINL	ANI	0FH		LOW 4 BITS
00B9	C6	30		2370		ADI	48		ASCII BIAS
00BB	FE	3A		2380		CPI	58		DIGIT 0-9
00BD	DA	2C	00	2390		JC	PTCN		
00C0	C6	07		2400		ADI	7		DIGIT A-F
00C2	C3	2C	00	2410		JMP	PTCN		
00C5	7B			3000	BMP	MOV	A,E		
00C6	95			3010		SUB	L		
00C7	C2	CC	00	3020		JNZ	GOON		
00CA	7A			3030		MOV	A,D		
00CB	9C			3040		SBB	H		
00CC	23			3050	GOON	INX	H		
00CD	C9			3060		RET			

SYMBOL TABLE

AHE1	0013	AHEX	000E	ALF	0023	BINH	00B3	BINL	00B7	BMP	00C5
CONC	0000	COND	0001	CRLF	0038	CYCL	0059	ERR	009F	GOON	00CC
PEVE	0089	PT2	00AB	PTAD	0090	PTCN	002C	PTLOP	002D	RDCN	0042
RLOP	006E	RNDM	0081	SPCE	002A	SPTR	0100	START	0000	TLOP	005F
TMEM	0050										

\$D 4000 40CF

4000	31	00	01	CD	38	00	3E	2A	CD	2C	00	C3	50	00	21	00
4010	00	0E	04	CD	42	00	29	29	29	D6	30	FE	0A	DA	23	
4020	00	D6	07	85	6F	0D	C2	13	00	EB	3E	20	F5	DB	00	E6
4030	80	C2	2D	00	F1	D3	01	C9	3E	0D	CD	2C	00	3E	0A	C3
4040	2C	00	DB	00	E6	01	C2	42	00	DB	01	E6	7F	C3	2C	00
4050	CD	0E	00	CD	0E	00	01	5A	5A	CD	81	00	C5	E5	D5	CD
4060	81	00	70	CD	C5	00	C2	5F	00	D1	E1	C1	E5	D5	CD	81
4070	00	7E	B8	C4	9F	00	CD	C5	00	C2	6E	00	D1	E1	C3	59
4080	00	78	E6	B4	A7	EA	89	00	37	79	17	4F	78	17	47	C9
4090	CD	38	00	7C	CD	AB	00	7D	CD	AB	00	CD	2A	00	C9	F5
40A0	CD	90	00	78	CD	AB	00	CD	2A	00	F1	F5	CD	B3	00	F1
40B0	C3	B7	00	1F	1F	1F	1F	E6	0F	C6	30	FE	3A	DA	2C	00
40C0	C6	07	C3	2C	00	7B	95	C2	CC	00	7A	9C	23	C9	00	00

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ERROR MAPPING MEMORY TEST

THE ERROR MAPPING MEMORY TEST ON THE FOLLOWING PAGES IS USEFUL SINCE IT PROVIDES A MAP OF THE MEMORY BOARD ON THE DISPLAY AND INDICATES THE EXACT BOARD LOCATION OF BAD MEMORY CHIPS. THIS PROGRAM IS WRITTEN TO MAP VECTOR GRAPHIC 8K AND 16K STATIC MEMORY BOARDS. NOTE THAT THE PROGRAM REQUIRES SPECIFIC EQUIPMENT FOR OPERATION (LISTED AT BEGINNING OF PROGRAM LISTING).

ADDR	B1	B2	B3	E	LINE	LABEL	OPCD	OPERAND
0000					0010	*ERROR MAPPING MEMORY TEST ROUTINE		
0000					0020	* R.S.HARP 2/17/78		
0000					0030	* EQUIPMENT REQUIRED:		
0000					0040	* EXTENDED MONITOR		
0000					0050	* FLASHWRITER AT D000		
0000					0060	* 8K MEMORY TESTED FROM 0000 TO 1FFF		
0000					0070	* 16K MEMORY TESTED FROM 8000 TO BFFF		
0000	DFDB				0080	CURS	EQU	ODFDBH CURSOR LOC FOR 2708 P/ R
0000					0090		ORG	2A00H
2A00	CD	2B	2C		0100	START	CALL	CLRSCRN
2A03	21	D2	2A		0110		LXI	H,MSG1
2A06	CD	0A	2C		0120		CALL	MSGPT
2A09	21	F7	2A		0123		LXI	H,MSG3
2A0C	CD	0A	2C		0125		CALL	MSGPT
2A0F	21	08	2B		0127		LXI	H,MSG2
2A12	CD	0A	2C		0129		CALL	MSGPT
2A15	CD	BD	C0		0130		CALL	RDCN
2A18	FE	34			0140		CPI	'4'
2A1A	CA	74	2B		0150		JZ	FORK
2A1D	FE	31			0160		CPI	'1' 1K RAM
2A1F	C2	00	2A		0170		JNZ	START NOT VALID ENTRY
2A22	21	4E	2B		0172	ONEK	LXI	H,MSG5
2A25	CD	0A	2C		0174		CALL	MSGPT
2A28	CD	1D	2C		0175		CALL	HMCURS
2A2B	3E	20			0180		MVI	A,020H
2A2D	32	E1	DF		0190		STA	INCRM FIX NO OF DOTS
2A30	CD	87	2A		0200		CALL	MATRX PLOT DOT ARRAY
2A33	CD	1D	2C		0210		CALL	HMCURS
2A36	21	00	00		0220		LXI	H,0
2A39	22	E2	DF		0230		SHLD	CYCLS
2A3C	11	FF	1F		0240		LXI	D,1FFFH TOP OF MEMORY
2A3F	01	5A	5A		0250		LXI	B,5A5AH SEED
2A42	2A	E2	DF		0260	MEMT	LHLD	CYCLS
2A45	23				0270		INX	H
2A46	22	E2	DF		0280		SHLD	CYCLS
2A49	3E	D1			0290		MVI	A,0D1H
2A4B	32	DC	DF		0300		STA	CURS+1
2A4E	AF				0310		XRA	A
2A4F	32	DB	DF		0320		STA	CURS
2A52	CD	B9	C1		0330		CALL	PTAD+3 PRINT NO OF CYCLES
2A55	CD	1D	2C		0350		CALL	HMCURS
2A58	21	00	00		0370		LXI	H,0 START OF MEMORY
2A5B	CD	A7	C1		0380		CALL	RNDM
2A5E	C5				0390		PUSH	B
2A5F	E5				0400		PUSH	H
2A60	CD	A7	C1		0410	TLOP	CALL	RNDM
2A63	70				0420		MOV	M,B
2A64	CD	54	C2		0430		CALL	BMP
2A67	C2	60	2A		0440		JNZ	TLOP
2A6A	E1				0450		POP	H
2A6B	C1				0460		POP	B
2A6C	CD	A7	C1		0470	RLOP	CALL	RNDM
2A6F	7E				0480		MOV	A,M
2A70	B8				0490		CMP	B
2A71	CA	7B	2A		0500		JZ	NOERR
2A74	E5				0510		PUSH	H
2A75	C5				0520		PUSH	B
2A76	CD	AC	2A		0530		CALL	PLOT8

ADDR	B1	B2	B3	E	LINE	LABEL	OPCD	OPERAND
2A79	C1				0540		POP	B
2A7A	E1				0550		POP	H
2A7B	CD	54	C2		0560	NOERR	CALL	BMP
2A7E	C2	6C	2A		0570		JNZ	RLOP
2A81	CD	CD	CO		0580		CALL	PAUSE
2A84	C3	42	2A		0590		JMP	MEMT
2A87					0600	* MATRIX PLOT	8 X 8	ARRAY OF DOTS
2A87	21	00	D2		0610	MATRX	LXI	H,OD200H
2A8A	36	2E			0620		MVI	M,'.'
2A8C	23				0630		INX	H
2A8D	36	20			0640		MVI	M,20H
2A8F	23				0650		INX	H
2A90	36	20			0660		MVI	M,20H
2A92	23				0670		INX	H
2A93	36	20			0680		MVI	M,20H
2A95	23				0690		INX	H
2A96	7D				0700		MOV	A,L
2A97	E6	20			0710		ANI	20H
2A99	CA	8A	2A		0720		JZ	MATRX+3
2A9C	3A	E1	DF		0730		LDA	INCRM
2A9F	85				0740		ADD	L
2AA0	6F				0750		MOV	L,A
2AA1	D2	A5	2A		0760		JNC	NCAR
2AA4	24				0770		INR	H
2AA5	7C				0780	NCAR	MOV	A,H
2AA6	FE	D4			0790		CPI	OD4H
2AA8	C2	8A	2A		0800		JNZ	MATRX+3
2AAB	C9				0810		RET	
2AAC					0820	* PLOT AN X FOR EVERY	BAD BIT	
2AAC	F5				0830	PLOT8	PUSH	PSW
2AAD	7C				0840		MOV	A,H
2AAE	E6	1C			0850		ANI	01CH
2AB0	17				0860		RAL	
2AB1	17				0870		RAL	
2AB2	17				0880		RAL	
2AB3	17				0890		RAL	
2AB4	5F				0900		MOV	L,A
2AB5	3E	00			0910		MVI	A,0
2AB7	CE	D2			0920		ACI	OD2H START OF TABLE
2AB9	67				0930		MOV	H,A HL CONT START OF LINE
2ABA	F1				0940		POP	PSW
2ABB	90				0950		SUB	B
2ABC	D2	C1	2A		0960		JNC	CONTP A>B
2ABF	2F				0970		CMA	
2AC0	3C				0980		INR	A
2AC1	06	09			0990	CONTP	MVI	B,9 PLOT 8 LOCATIONS
2AC3	05				1000		DCR	B
2AC4	C8				1010		RZ	PLOT FINISHED
2AC5	17				1020		RAL	
2AC6	D2	CB	2A		1030		JNC	NERR BIT OK
2AC9	36	58			1040		MVI	M,'X' PLOT ERROR
2ACB	23				1050	NERR	INX	H
2ACC	23				1060		INX	H
2ACD	23				1070		INX	H
2ACE	23				1080		INX	H
2ACF	C3	C3	2A		1090		JMP	CONTP+2
2AD2					1100	* MESSAGES		
2AD2	0A	DO			1105	MSG1	DW	OD00AH

ADDR	B1	B2	B3	E	LINE	LABEL	OPCD	OPERAND
2AD4	56	45	43		1110		DTZ	'VECTOR GRAPHIC MEMORY TEST P ROGRAM'
2AD7	54	4F	52					
2ADA	20	47	52					
2ADD	41	50	48					
2AE0	49	43	20					
2AE3	4D	45	4D					
2AE6	4F	52	59					
2AE9	20	54	45					
2AEC	53	54	20					
2AEF	50	52	4F					
2AF2	47	52	41					
2AF5	4D	00						
2AF7	80	D0			1120	MSG3	DW	OD080H
2AF9	31	4B	20		1130		DTZ	'1K RAM OR 4K?'
2AFC	52	41	4D					
2AFF	20	4F	52					
2B02	20	34	4B					
2B05	3F	00						
2B07	00				1140		NOP	
2B08	00	D1			1145	MSG2	DW	OD100H
2B0A	30	30	30		1150		DTZ	'0000 TEST CYCLES COMPLETED'
2B0D	30	20	20					
2B10	54	45	53					
2B13	54	20	43					
2B16	59	43	4C					
2B19	45	53	20					
2B1C	43	4F	4D					
2B1F	50	4C	45					
2B22	54	45	44					
2B25	00							
2B26	00				1160		DB	0
2B27	80	D0			1165	MSG4	DW	OD080H
2B29	31	36	4B		1167		DTZ	'16K RAM UNDER TEST FROM 8000 TO BFFF'
2B2C	20	52	41					
2B2F	4D	20	55					
2B32	4E	44	45					
2B35	52	20	54					
2B38	45	53	54					
2B3B	20	46	52					
2B3E	4F	4D	20					
2B41	38	30	30					
2B44	30	20	54					
2B47	4F	20	42					
2B4A	46	46	46					
2B4D	00							
2B4E	80	D0			1168	MSG5	DW	OD080H
2B50	38	4B	20		1169		DTZ	'8K RAM UNDER TEST FROM 0000 TO 1FFF'
2B53	52	41	4D					
2B56	20	55	4E					
2B59	44	45	52					
2B5C	20	54	45					
2B5F	53	54	20					
2B62	46	52	4F					
2B65	4D	20	30					
2B68	30	30	30					
2B6B	20	54	4F					
2B6F	20	21	46					

ADDR	B1	B2	B3	E	LINE	LABEL	OPCD	OPERAND
2B74					1170	* MONITOR ROUTINES		
2B74		C254			1180	BMP	EQU	OC254H
2B74		C1B6			1190	PTAD	EQU	OC1B6H
2B74		C1A7			1200	RNDM	EQU	OC1A7H
2B74		COCD			1210	PAUSE	EQU	OCOCDH
2B74		DFE1			1220	INCRM	EQU	CURS+6
2B74		DFE2			1230	CYCLS	EQU	CURS+7
2B74		COBD			1240	RDCN	EQU	OCOBDH
2B74		C098			1250	PTCN	EQU	OC098H
2B74					1260	* ROUTINES FOR 16K RAM		
2B74	21	27	2B		1264	FORK	LXI	H,MSG4
2B77	CD	0A	2C		1264		CALL	MSGPT
2B7A	CD	1D	2C		1265		CALL	HMCURS
2B7D	3E	60			1270		MVI	A,60H
2B7F	32	E1	DF		1280		STA	INCRM
2B82	CD	87	2A		1290		CALL	MATRX
2B85	3E	08			1300		MVI	A,8
2B87	CD	98	C0		1310		CALL	PTCN
2B8A	21	00	00		1320		LXI	H,0
2B8D	22	E2	DF		1330		SHLD	CYCLS
2B90	11	FF	BF		1340		LXI	D,0BFFFH END OF BLOCK
2B93	01	5A	5A		1350		LXI	B,5A5AH SEED
2B96	2A	E2	DF		1360	MEMT4	LHLD	CYCLS
2B99	23				1370		INX	H
2B9A	22	E2	DF		1380		SHLD	CYCLS
2B9D	3E	D1			1390		MVI	A,0D1H
2B9F	32	DC	DF		1400		STA	CURS+1
2BA2	AF				1410		XRA	A
2BA3	32	DB	DF		1420		STA	CURS
2BA6	CD	B9	C1		1430		CALL	PTAD+3
2BA9	CD	1D	2C		1450		CALL	HMCURS
2BAC	21	00	80		1470		LXI	H,8000H START OF BLOCK
2BAF	CD	A7	C1		1480		CALL	RNDM
2BB2	C5				1490		PUSH	B
2BB3	E5				1500		PUSH	H
2BB4	CD	A7	C1		1510	TLOP4	CALL	RNDM
2BB7	70				1520		MOV	M,B
2BB8	CD	54	C2		1530		CALL	BMP
2BBB	C2	B4	2B		1540		JNZ	TLOP4
2BBE	E1				1550		POP	H
2BBF	C1				1560		POP	B
2BC0	CD	A7	C1		1570	RLOP4	CALL	RNDM
2BC3	7E				1580		MOV	A,M
2BC4	B8				1590		CMP	B
2BC5	CA	CF	2B		1600		JZ	NERR4
2BC8	E5				1610		PUSH	H
2BC9	C5				1620		PUSH	B
2BCA	CD	DB	2B		1630		CALL	PLT16
2BCD	C1				1640		POP	B
2BCE	E1				1650		POP	H
2BCF	CD	54	C2		1660	NERR4	CALL	BMP
2BD2	C2	C0	2B		1670		JNZ	RLOP4
2BD5	CD	CD	C0		1680		CALL	PAUSE
2BD8	C3	96	2B		1690		JMP	MEMT4
2BDB					1700	* PLOT ERRORS FOR 16K BOARD		
2BDB	F5				1710	PLT16	PUSH	PSW
2BDC	CD	F9	2B		1720		CALL	SCLOC
2BDF	F1				1730		POP	PSW

ADDR	B1	B2	B3	E	LINE	LABEL	OPCD	OPERAND
2BE0	90				1740		SUB	B
2BE1	D2	E6	2B		1750		JNC	AGTB
2BE4	2F				1760		CMA	
2BE5	3C				1770		INR	A
2BE6	F5				1780	AGTB	PUSH	PSW
2BE7	E6	0F			1790		ANI	15
2BE9	CA	EE	2B		1800		JZ	CON16
2BEC	36	58			1810		MVI	M, 'X'
2BEE	7D				1820	CON16	MOV	A, L
2BEF	C6	80			1830		ADI	80H
2BF1	6F				1840		MOV	L, A
2BF2	F1				1850		POP	PSW
2BF3	E6	F0			1860		ANI	0F0H
2BF5	C8				1870		RZ	
2BF6	36	58			1880		MVI	M, 'X'
2BF8	C9				1890		RET	
2BF9	7C				1900	SCLOC	MOV	A, H
2BFA	F5				1910		PUSH	PSW
2BFB	2F				1920		CMA	
2BFC	E6	1C			1930		ANI	1CH
2BFE	6F				1940		MOV	L, A
2BFF	F1				1950		POP	PSW
2C00	E6	20			1960		ANI	20H
2C02	17				1970		RAL	
2C03	17				1980		RAL	
2C04	17				1990		RAL	
2C05	17				2000		RAL	
2C06	C6	D2			2010		ADI	0D2H
2C08	67				2020		MOV	H, A
2C09	C9				2030		RET	
2COA					2040	* MESSAGE PRINTING ROUTINE		
2COA	D5				2050	MSGPT	PUSH	D
2COB	5E				2051		MOV	E, M
2COC	23				2052		INX	H
2COD	56				2053		MOV	D, M
2COE	23				2054		INX	H
2COF	EB				2055		XCHG	
2C10	1A				2056	MSLOP	LDAX	D
2C11	A7				2058		ANA	A
2C12	CA	1B	2C		2059		JZ	RETUR
2C15	77				2060		MOV	M, A
2C16	23				2061		INX	H
2C17	13				2062		INX	D
2C18	C3	10	2C		2063		JMP	MSLOP
2C1B	D1				2064	RETUR	POP	D
2C1C	C9				2065		RET	
2C1D					2110	* HOME THE CURSOR		
2C1D	E5				2120	HMCURS	PUSH	H
2C1E	2A	DB	DF		2140		LHLD	CURS
2C21	36	20			2150		MVI	M, 20H
2C23	21	00	DO		2160		LXI	H, 0D000H
2C26	22	DB	DF		2170		SHLD	CURS
2C29	E1				2180		POP	H
2C2A	C9				2190		RET	
2C2B					2200	* CLEAR THE SCREEN		
2C2B	21	00	DO		2210	CLRSCRN	LXI	H, 0D000H
2C2E	36	20			2220		MVI	M, 20H
2C30	23				2225		INX	H

ADDR	B1	B2	B3	E	LINE	LABEL	OPCD	OPERAND
2C31	7C				2230		MOV	A,H
2C32	FE	D8			2240		CPI	OD8H
2C34	C2	2E	2C		2250		JNZ	CLRSCRN+3
2C37	C3	1D	2C		2260		JMP	HMCURS
2C3A					2270		END	START

2A00 CD 2B 2C 21 D2 2A CD 0A 2C 21 F7 2A CD 0A 2C 21
 2A10 08 2B CD 0A 2C CD BD C0 FE 34 CA 74 2B FE 31 C2
 2A20 00 2A 21 4E 2B CD 0A 2C CD 1D 2C 3E 20 32 E1 DF
 2A30 CD 87 2A CD 1D 2C 21 00 00 22 E2 DF 11 FF 1F 01
 2A40 5A 5A 2A E2 DF 23 22 E2 DF 3E D1 32 DC DF AF 32
 2A50 DB DF CD B9 C1 CD 1D 2C 21 00 00 CD A7 C1 C5 E5
 2A60 CD A7 C1 70 CD 54 C2 C2 60 2A E1 C1 CD A7 C1 7E
 2A70 B8 CA 7B 2A E5 C5 CD AC 2A C1 E1 CD 54 C2 C2 6C
 2A80 2A CD CD C0 C3 42 2A 21 00 D2 36 2E 23 36 20 23
 2A90 36 20 23 36 20 23 7D E6 20 CA 8A 2A 3A E1 DF 85
 2AA0 6F D2 A5 2A 24 7C FE D4 C2 8A 2A C9 F5 7C E6 1C
 2AB0 17 17 17 17 6F 3E 00 CE D2 67 F1 90 D2 C1 2A 2F
 2AC0 3C 06 09 05 C8 17 D2 CB 2A 36 58 23 23 23 23 C3
 2AD0 C3 2A 0A D0 56 45 43 54 4F 52 20 47 52 41 50 48
 2AE0 49 43 20 4D 45 4D 4F 52 59 20 54 45 53 54 20 50
 2AF0 52 4F 47 52 41 4D 00 80 D0 31 4B 20 52 41 4D 20
 2B00 4F 52 20 34 4B 3F 00 00 00 D1 30 30 30 30 20 20
 2B10 54 45 53 54 20 43 59 43 4C 45 53 20 43 4F 4D 50
 2B20 4C 45 54 45 44 00 00 80 D0 31 36 4B 20 52 41 4D
 2B30 20 55 4E 44 45 52 20 54 45 53 54 20 46 52 4F 4D
 2B40 20 38 30 30 30 20 54 4F 20 42 46 46 46 00 80 D0
 2B50 38 4B 20 52 41 4D 20 55 4E 44 45 52 20 54 45 53
 2B60 54 20 46 52 4F 4D 20 30 30 30 30 20 54 4F 20 31
 2B70 46 46 46 00 21 27 2B CD 0A 2C CD 1D 2C 3E 60 32
 2B80 E1 DF CL 87 2A 3E 08 CD 98 C0 21 00 00 22 E2 DF
 2B90 11 FF BF 01 5A 5A 2A E2 DF 23 22 E2 DF 3E D1 32
 2BA0 DC DF AF 32 DB DF CD B9 C1 CD 1D 2C 21 00 80 CD
 2BB0 A7 C1 C5 E5 CD A7 C1 70 CD 54 C2 C2 B4 2B E1 C1
 2BC0 CD A7 C1 7E B8 CA CF 2B E5 C5 CD DB 2B C1 E1 CD
 2BD0 54 C2 C2 C0 2B CD CD C0 C3 96 2B F5 CD F9 2B F1
 2BE0 90 D2 E6 2B 2F 3C F5 E6 OF CA EE 2B 36 58 7D C6
 2BF0 80 6F F1 E6 F0 C8 36 58 C9 7C F5 2F E6 1C 6F F1
 2C00 E6 20 17 17 17 17 C6 D2 67 C9 D5 5E 23 56 23 EB
 2C10 1A A7 CA 1B 2C 77 23 13 C3 10 2C D1 C9 E5 2A DB
 2C20 DF 36 20 21 00 D0 22 DB DF E1 C9 21 00 D0 36 20
 2C30 23 7C FE D8 C2 2E 2C C3 1D 2C

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TROUBLE SHOOTING

IF YOU HAVE CHECKED THE MEMORY SOCKETS FOR SHORT CIRCUITS AND ARE STILL HAVING TROUBLE, CONSIDERABLE INFORMATION CAN BE GAINED FROM THE MEMORY TEST PROGRAM PRINT OUT. IF A SMALL NUMBER OF MEMORY LOCATIONS ARE BAD, CONVERT TO HEX TO FIND THE ROW WITH THE BAD CHIP USING THE COMPONENT PLACEMENT DIAGRAM AS A GUIDE. THE DIFFERENCE BETWEEN WHAT WAS WRITTEN AND WHAT WAS READ INDICATES WHICH BIT IS BAD. FOR EXAMPLE, IF THE DIFFERENCE IS 128, THEN BIT 7 IS BAD. TURN OFF THE POWER AND REPLACE THE INDICATED CHIP.

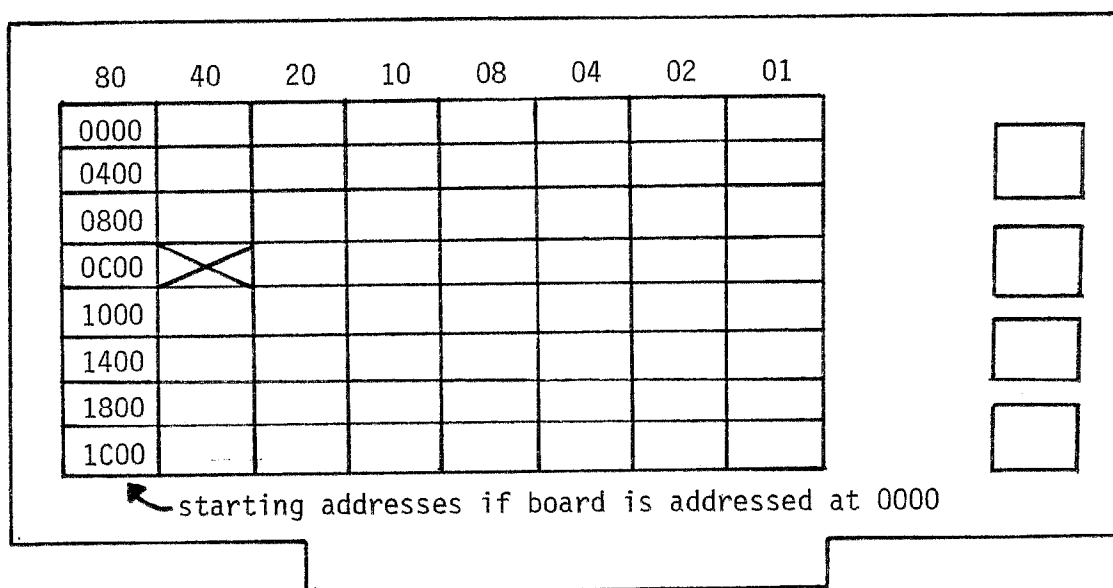
IF BLOCKS LARGER THAN 1K INDICATE BAD, CHECK THE PROTECT SWITCH. SOLDER FLUX OR DIRT SOMETIMES MAKES THE SWITCH ERRATIC. THE SAME IS TRUE OF THE ADDRESS SELECT SWITCHES.

IF YOU ARE STILL HAVING TROUBLE, REMOVE THE BOARD AND CAREFULLY EXAMINE IT WITH A MAGNIFYING GLASS FOR SOLDER BRIDGES. THE NEXT STEP REQUIRES AN EXTENDER BOARD, AND EITHER A LOGIC PROBE OR SCOPE. IN THE TEST PROGRAM DELETE LINES 150, 160, 170, 190 AND 210 AND REPLACE LINE 180 WITH D=PEEK (N). THIS WILL CAUSE THE PROGRAM TO EXERCISE THE MEMORY READ AND WRITE CIRCUITRY. TRACE THROUGH THE CIRCUITRY STARTING WITH THE 74LS42 OUTPUTS TO FIND THE PROBLEM.

8K MEMORY USERS GUIDE

HOW TO LOCATE BAD MEMORY CHIPS

DEFECTS IN MEMORY COMPONENTS CAN REVEAL THEMSELVES EITHER WHEN THE BOARD IS FIRST TESTED, OR AFTER HOURS OF OPERATION. THERMALLY INTERMITTENT PROBLEMS MAY OCCUR WHEN THE BOARD IS HOT, OR ONLY WHEN THE SYSTEM IS FIRST TURNED ON. DEFECTS IN THE ON CHIP ADDRESS DECODERS OR ADJACENT MEMORY CELLS CAN OCCUR SUCH THAT EACH MEMORY LOCATION APPEARS TO WORK PROPERLY WHEN TESTED BY ITSELF, BUT WRITING IN ANOTHER MEMORY LOCATION WILL CAUSE IT TO CHANGE. INPUT SHORTS MAY CAUSE ONE BAD CHIP TO DISABLE THE ENTIRE BOARD. SMALL BLOCKS OF MEMORY THAT TEST BAD IN ONLY ONE BIT CAN BE READILY ISOLATED WITH THE FOLLOWING CHART.



RUN THE MACHINE LANGUAGE MEMORY TEST PROGRAM WITH THE BOARD ADDRESSED AT SOME CONVENIENT LOCATION SUCH AS 2000, OR IF YOU HAVE THE VECTOR 1 MONITOR, TYPE T 2000 3FFF. IF ERRORS ARE DETECTED, THEY WILL BE PRINTED OUT IN A FEW SECONDS. BY WAY OF EXAMPLE, ASSUME THE FOLLOWING IS OBTAINED:

* T 2000 3FFF

```
2C02    47  87
2C04    D3  93
2D05    13  53
2E08    89  C9
2F15    32  72
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ALL OF THESE LOCATIONS ARE IN THE SAME 1K BLOCK, THE FOURTH ROW OF CHIPS ON THE DIAGRAM, SINCE THE BOARD ADDRESS IS 2000. IT IS ALSO APPARENT THAT THE ABSOLUTE DIFFERENCE BETWEEN THE NUMBER WRITTEN INTO MEMORY AND THAT READ FROM MEMORY IS 40 HEX. THIS MEANS THE DEFECTIVE CHIP IS IN THE COLUMN OF CHIPS LABELED 40 AS INDICATED BY THE X.

GENERAL TROUBLE SHOOTING GUIDE

BECAUSE OF THE COMPLEXITY OF THE ENTIRE COMPUTER SYSTEM, BOTH HARDWARE AND SOFTWARE, IT IS ESSENTIAL TO ISOLATE ANY PROBLEM TO AN INDIVIDUAL BOARD OR PROGRAM. FORTUNATELY, ALL OF THE COMPUTER LOGIC IS ON EASILY REMOVABLE BOARDS. IT IS EXTREMELY VALUABLE TO HAVE ACCESS TO A TESTED COMPUTER SO THAT THE BOARDS CAN BE INDIVIDUALLY TESTED. ALTHOUGH THERE IS THE POSSIBILITY OF INTERACTION BETWEEN BOARDS DUE TO MARGINAL TIMING OR DEFECTIVE COMPONENTS, THIS IS NOT THE USUAL CASE, AND IT IS BEST TO ASSUME THAT IF A BOARD WORKS IN COMPUTER "A" IT WILL ALSO WORK IN COMPUTER "B".

THE MINIMUM SYSTEM CONSISTS OF THREE BOARDS: THE CPU BOARD, THE PROM/RAM BOARD, AND EITHER A VIDEO OR SERIAL I/O BOARD. MAKE SURE THAT THE MONITOR PROGRAM HAS BEEN PROPERLY PATCHED FOR THE PARTICULAR I/O CONFIGURATION OF YOUR SYSTEM. THERE IS TOTAL CONFUSION IN THE INDUSTRY CONCERNING PORT ASSIGNMENTS, LOGIC CONVENTIONS, AND STRAPPING OPTIONS. SEVERAL TYPES OF PROGRAMMABLE USARTS ARE USED WHICH REQUIRE INITIALIZATION.

IF YOU HAVE CAREFULLY FOLLOWED THE ASSEMBLY INSTRUCTIONS FOR EACH OF THE BOARDS AND THE REGULATORS CHECK OUT, INSTALL ALL CHIPS. LET'S ASSUME YOU ARE USING A VIDEO DISPLAY. AS SOON AS YOU TURN THE COMPUTER ON, YOU SHOULD SEE A DISPLAY OF RANDOM MEMORY GARBAGE ON THE TV SCREEN. THIS WILL BE INDEPENDENT OF ANY FUNCTIONING OF THE COMPUTER OTHER THAN THE CLOCK OSCILLATOR. IF YOU DO NOT GET A PROPER DISPLAY, THE VIDEO INTERFACE MUST BE DEBUGGED FIRST. FEEL THE CHIPS ON THE BOARD. ANY THAT ARE HOT TO THE TOUCH MAY BE IN BACKWARD (PROBABLY DESTROYED IF TTL) OR MAY HAVE THEIR OUTPUTS SHORTED. THERE IS MORE THAN A FACTOR OF TEN DIFFERENCE IN THE POWER DISSIPATION OF TTL CHIPS, BUT THEY SHOULD NOT BE UNCOMFORTABLY HOT TO THE TOUCH.

REMOVE THE BOARD AND INSPECT IT CAREFULLY. ABOUT HALF OF THE PROBLEMS CAN BE FOUND SIMPLY BY VISUAL INSPECTION. LOOK WITH A MAGNIFYING GLASS OR INSPECTION SCOPE AT EACH PIN ON THE BOTTOM FOR UNSOLDERED PINS, MISSING PINS THAT MAY BE BENT UNDER OR BROKEN OFF, SOLDER BRIDGES BETWEEN PINS OR TO ADJACENT TRACES, AND ETCH BRIDGES BETWEEN TRACES (VERY HARD TO SEE). A CAREFUL EXAMINATION WILL TAKE 15 MINUTES, BUT MAY SAVE YOU A LOT OF GRIEF, AND YOU MAY DISCOVER PROBLEMS LIKE UNSOLDERED PINS THAT MAY REVEAL THEMSELVES ONLY LATER AS INTERMITTENT PROBLEMS. EXAMINE THE TOP OF THE BOARD TO BE SURE THE PROPER CHIPS ARE INSTALLED IN THE RIGHT PLACES. SIGHT ALONG THE EDGE OF THE CHIPS TO FIND BENT UNDER PINS. CHIPS ARE SOMETIMES INSERTED WITH A WHOLE ROW OF PINS THAT MISS THE SOCKET HOLES.

IF THE VISUAL INSPECTION FAILS TO GET THE VIDEO DISPLAY WORKING, A COMPONENT MAY BE BAD (USUALLY AN IC). TRY EXCHANGING IDENTICAL COMPONENTS TO SEE IF THE SYMPTOMS CHANGE. AT THIS POINT IT IS WISE TO GO BACK AND CAREFULLY REREAD THE MANUAL TO BE SURE YOU UNDERSTAND THE WAY THE BOARD WORKS AND THAT YOU HAVE SELECTED THE PROPER JUMPER OPTIONS. AFTER THIS, YOU WILL PROBABLY WANT TO TAKE THE UNIT TO A DEALER IF YOU ARE NOT FAMILIAR WITH DIGITAL TROUBLE SHOOTING PROCEDURES, OR GO THROUGH THE CIRCUIT BLOCK BY BLOCK WITH A SCOPE OR LOGIC PROBE IF YOU ARE EXPERIENCED.

AFTER THE VIDEO DISPLAY OR SERIAL I/O IS WORKING, THE RESET SWITCH SHOULD CAUSE A "*" PROMPT TO BE WRITTEN. IF THIS DOES NOT WORK, FOLLOW THE SAME PROCEDURE ON THE CPU AND PROM/RAM BOARDS. THE CPU BOARD CONSISTS MOSTLY OF 8097 BUS DRIVERS

WHICH CAN BE EXCHANGED ONE BY ONE. THE VECTORED INTERRUPT AND REAL TIME CLOCK COMPONENTS, IC A1, ARE NOT NECESSARY IN THE BOARD AT THIS TIME AND SHOULD BE REMOVED. USING A SCOPE, EXAMINE THE OUTPUT PINS OF ALL CHIPS. LOW LOGIC LEVELS ARE NORMALLY LESS THAN 0.2 VOLTS AND HIGH GREATER THAN 3.0 VOLTS. A LEVEL OF 0.4 VOLTS MAY INDICATE SHORTS BETWEEN OUTPUTS WHERE ONE IS TRYING TO PULL HIGH AND THE OTHER LOW. A LEVEL OF 1.2 VOLTS INDICATES AN OPEN CIRCUITED INPUT. NMOS CHIPS HAVE SIMILAR LOGIC LEVELS, WHILE PMOS CHIPS CAN PULL TTL INPUTS TO -0.6V WHERE THE INPUT CLAMP DIODE LIMITS THE VOLTAGE. DO NOT BE SURPRISED AT HOW STRANGE SOME OF THE WAVEFORMS ON THE BUS LOOK, SUCH AS THE DI LINES. THERE ARE PERIODS OF TIME DURING WHICH THE BUS IS NOT BEING ACTIVELY DRIVEN, AND THE VOLTAGE MAY DRIFT DUE TO RECEIVER INPUT CURRENT. ABNORMAL OPERATION IS INDICATED PRINCIPALLY BY ABNORMAL LOGIC LEVELS MAINTAINED CONSTANT FOR AT LEAST ONE CLOCK PERIOD (500 MICROSECONDS).

ONCE YOUR BASIC SYSTEM IS WORKING, CHECK OUT OF MEMORY BOARDS AND OTHER INTERFACES IS RELATIVELY STRAIGHTFORWARD USING THE MEMORY TEST PROGRAM IN THE MONITOR, OR SIMPLE DIAGNOSTIC ROUTINES YOU CAN PROGRAM IN MEMORY ON THE PROM/RAM BOARD. AFTER YOUR SYSTEM IS UP AND RUNNING, IT SHOULD BE QUITE RELIABLE. SINCE MOST MICROCOMPUTER SYSTEMS ARE MEMORY INTENSIVE, THE MEMORY IS THE MOST LIKELY SOURCE OF COMPONENT FAILURE. A SYSTEM WITH 32K OF STATIC MEMORY MAY CONTAIN 75% OF ITS COMPONENTS ON THE MEMORY BOARDS. IF A PROBLEM IS EXPERIENCED RUNNING A PROGRAM, FIRST SUSPECT THE MEMORY AND USE THE MONITOR TEST PROGRAM. WE HAVE YET TO EXPERIENCE A PROBLEM WITH OUR 8K MEMORY BOARDS THAT WAS NOT REVEALED BY THE TEST PROGRAM. IF YOU DO MUCH REARRANGING OF YOUR SYSTEM, IT IS A GOOD PRACTICE TO TEST MEMORY FOR A FEW SECONDS WHEN YOU FIRST TURN ON THE COMPUTER TO MAKE SURE THE BOARDS ARE ADDRESSED PROPERLY OR THAT THEY ARE IN THE COMPUTER. THIS MAY SAVE SOME HEAD SCRATCHING WHEN THE PROGRAM YOU HAVE JUST LOADED FAILS TO RESPOND TO YOUR EAGER KEYBOARD TOUCH. IF YOU SUSPECT TEMPERATURE SENSITIVE CHIPS, REMOVE THE COVER OF THE COMPUTER TO INTERRUPT AIR FLOW BETWEEN BOARDS. WE DO NOT RECOMMEND OBSTRUCTING THE AIR FLOW THROUGH THE COMPUTER BY PLACING A SHEET OF PAPER OVER THE LEFT SIDE. A FULL COMPUTER MAY DISSIPATE OVER 300 WATTS AND REACH UNACCEPTABLE TEMPERATURES IF NO AIRFLOW IS PERMITTED.

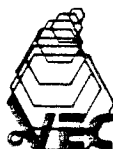
APPENDIX A ASCII CODE CHART

1968 ASCII: American Standard Code for Information Interchange. Standard No. X3.4-1968 of the American National Standards Institute.

Bits		b7 →	0	0	0	0	1	1	1	1	
		b6 →	0	0	1	1	0	0	1	1	
		b5 →	0	1	0	1	0	1	0	1	
b4 ↓	b3 ↓	b2 ↓	b1 ↓	COLUMN →		↓ ROW ↓					
				0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	@	P	'	p
0	0	0	1	1	SOH	DC1	!	A	Q	a	q
0	0	1	0	2	STX	DC2	"	B	R	b	r
0	0	1	1	3	ETX	DC3	#	C	S	c	s
0	1	0	0	4	EOT	DC4	\$	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	E	U	e	u
0	1	1	0	6	ACK	SYN	&	F	V	f	v
0	1	1	1	7	BEL	ETB	'	G	W	g	w
1	0	0	0	8	BS	CAN	(H	X	h	x
1	0	0	1	9	HT	EM)	I	Y	i	y
1	0	1	0	A	LF	SUB	*	J	Z	j	z
1	0	1	1	B	VT	ESC	+	K	[k	{
1	1	0	0	C	FF	FS	,	L	\	l	
1	1	0	1	D	CR	GS	-	M]	m	}
1	1	1	0	E	SO	RS	.	N	^	n	~
1	1	1	1	F	SI	US	/	O	_	o	DEL

All characters in these two columns and SP (Space) are non-printing.

When UPPER CASE ONLY is used, shaded lower case characters (columns 6 & 7) from keyboard are converted to their upper case equivalents (columns 4 & 5) before being printed or transmitted.



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